A HIGH POWER MIC PASSIVE DIODE RECEIVER PROTECTOR WITH INTEGRAL STC USING VARIABLE BASEWIDTH TECHNIQUES

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Abstract

A passive MIC receiver protector using graded diode basewidths has been developed that handles 200 watt RF pulses at 10 percent duty rates on a 1.5 x 1.75 x 0.025 inch alumina substrate. Leakage power and recovery period are under 20 mW peak spike, 10 mW peak flat, and 0.8 μs. Data on harmonic generation is included. Integral STC during the receive period is included with the associated MIC digital driver.

Discussion

Circuit

An all solid-state broadband receiver protector (RP) with integral STC and driver has been designed for L-band frequencies on an alumina substrate. The unit consists of three silicon diode limiter stages (figure 1), each using a different basewidth. The input PIN diode has an 8 μm base region width to handle the 200 watt peak, 10 percent duty pulse train; the second limiter is a zero-bias punchthrough 4 μm abrupt-profile step-recovery diode; and the final limiter is similar to the second stage but has a 2 μm basewidth.

The smaller basewidth of the third diode is required because RF power incident on this stage is relatively low. The low RF power level, which causes a relatively small electric field to develop across the 2 μm junction, still injects sufficient charge to cause a significant change in junction capacitance. The consequent variation in C_J provides RF isolation.

The 2 μm diode stage is designed to be biased by the driver shown in figure 2 to provide controlled RF attenuation during radar receiver for STC or AGC functions up to 20 dB. In the absence of bias, the 2 μm diode provides passive receiver protection.

Development

The input PIN diode controls three key parameters: the recovery period, the leakage power, and the power handling capability. An experimental study of this stage was made on a separate substrate to optimize these parameters; the results showed that a diode base region width smaller than 8 μm could not handle the required RF power level but gave excellent recovery and leakage characteristics. A PIN diode much larger than 8 μm could handle the required RF power level but caused excessive leakage and recovery period.

By using an 8 μm diode with quasi-active bias (see figure 1), it was possible to bring leakage power down while maintaining RF power handling at 200 watts peak, but the recovery time was excessive. Recovery time was reduced by placing a resistor, R1, in series with CR1 to discharge the 8 μm diode rapidly after the transmitter pulse terminates. This arrangement reduced the recovery time at full power to 0.9 μs. The current lost by the bleeder, R1, during the charging period (transmitter pulse period) was made up by paralleling an additional Schottky barrier diode with CR4.

The second stage (w_b = 4 μm) is a straightforward limiter, and the final stage (w_b = 2 μm) serves as a sensitive (approximately zero dBm turn-on) passive limiter during the transmit period plus controlled STC or AGC attenuator during receive. In this way, one achieves RF attenuation of the echo in front of the low noise amplifier without a penalty in insertion loss or noise figure.

Limiting

Figure 3 depicts the pulsed limiting characteristic for both spike and flat leakage. Figure 4 shows the limiting of the fundamental and the relative amplitudes of the second and third harmonics generated because of the diode nonlinearities. Conversion to the third harmonic was considerably stronger than to the second.

Achieving Lowest Zero-Bias Insertion Loss on Receive

One of the most important parameters of an RP is insertion loss, which must be kept as low as possible so as not to increase the system noise factor. A 0.5 dB loss and 1.2 VSWR were achieved over the 20 percent band. The low loss and low VSWR were obtained by using a unique fabrication technique described below.

Figure 5 illustrates the spoke bonding of the gold-plated copper puck used to reduce R_s to its lowest value in order to reach lowest loss. (This connection mates the N^+ diode side to the ground plane.)

In addition, lead lengths ℓ_1 and ℓ_2 shown in figure 6 were decreased, thus varying their inductances to resonate with the junction capacitance of the diode, yielding the lowest shunt conductance.

This relationship of capacitance C_J, lead inductances L_1 and L_2, and shunt conductance G_r is shown in the equivalent circuit of figure 7a. The relationship to insertion loss α_L is shown in figure 7b.

The oscillogram of figure 8 demonstrates the diode tuning; that is, the raising of the resonant frequency by shortening the leads.

Figure 9 depicts the low loss and low VSWR achieved over a 20 percent bandwidth. The 0.5 dB loss was reproducible provided care was exercised during fabrication.

A separate investigation was made of MIC mountable capacitors used as dc blocks in four places, as was shown in figure 1. It was found that a single capacitor yielded the following losses at 2 GHz:

Interdigitated finger capacitor	0.05 dB/unit
MIS capacitor	0.03 dB/unit
MOS capacitor	0.035 dB/unit

MOS capacitors were used because MIS types are still in the early prototype stage and their reliability was not ascertained.

Data

The parameters achieved for the receiver protector are listed in figure 10.

Summary

The receiver protector provides passive protection against pulses of up to 200 watts peak and 10 percent duty at L-band frequencies; it also provides integral STC attenuation of up to 20 dB with a digitally commanded driver.

The device uses variable base region techniques, with each diode optimized to match RF incident power at each stage. The use of a discharge resistor in the quasi-active high-power limiter decreased recovery time satisfactorily while allowing adequate current for rapid turn-on and low leakage. Also, the use of crossed bonding straps in conjunction with the diode resonating technique reduced shunt conductance and gave relatively low cold loss.

Application Note

This unit is now being tested on an Air Force low cost, miniaturized radar system. Twelve units have been produced and successfully evaluated in the laboratory. Figure 11 shows the RF circuit and the driver substrate.

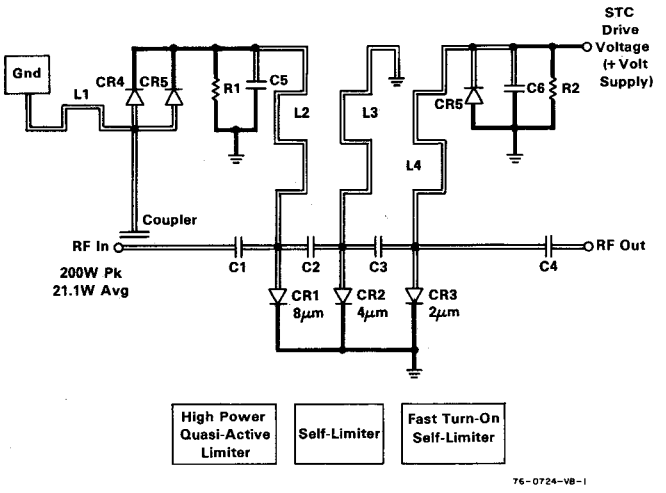

Figure 1. RF Circuit Schematic of WD 278 RP/STC

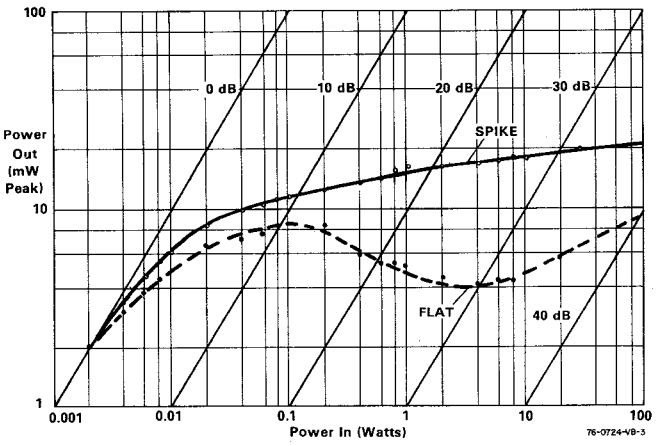

Figure 3. Limiting Characteristics

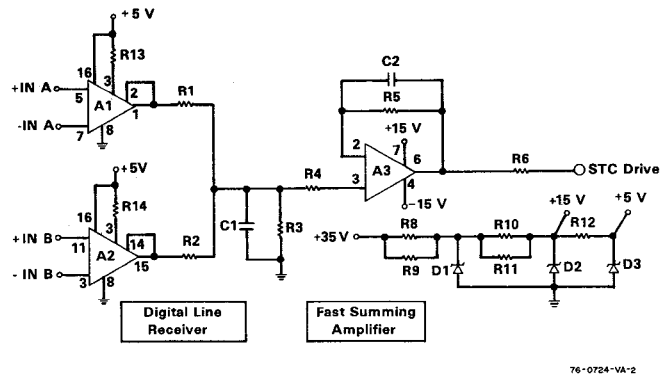

Figure 2. Digital Logic Driver Schematic

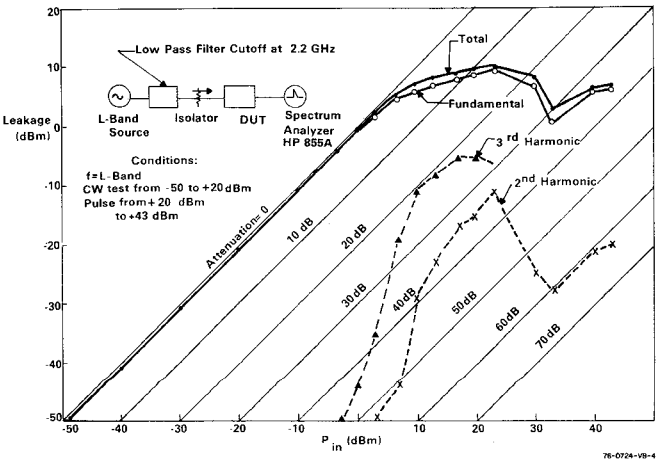

Figure 4. Harmonic Generation and Fundamental Frequency Limiting

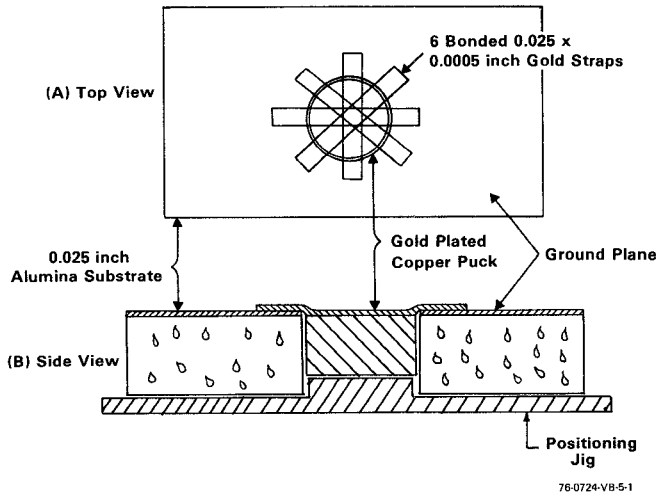

Figure 5. Details of Puck Mounting

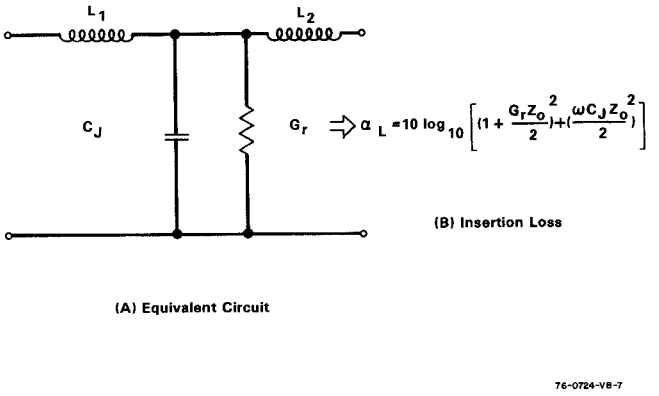

Figure 7. Shunt Mounted Diode Relationships at Zero Bias

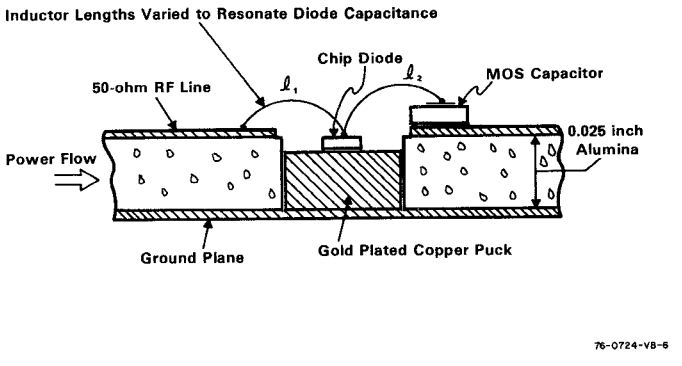

Figure 6. Diode Cross Section Showing Connecting Leads

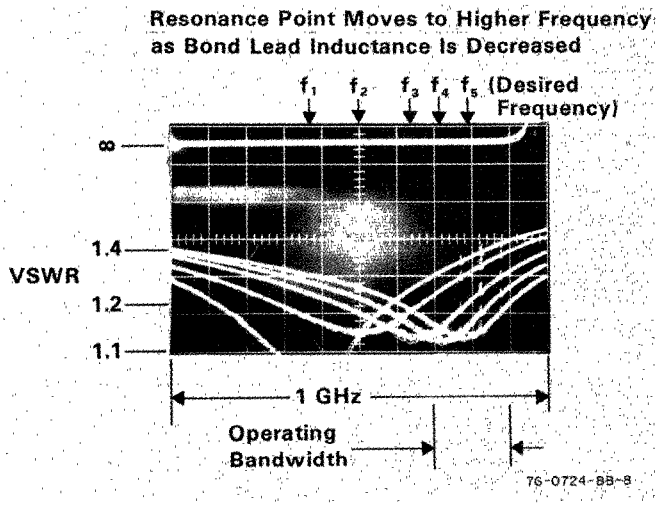

Figure 8. Tuning of a Single Shunt Diode Stage

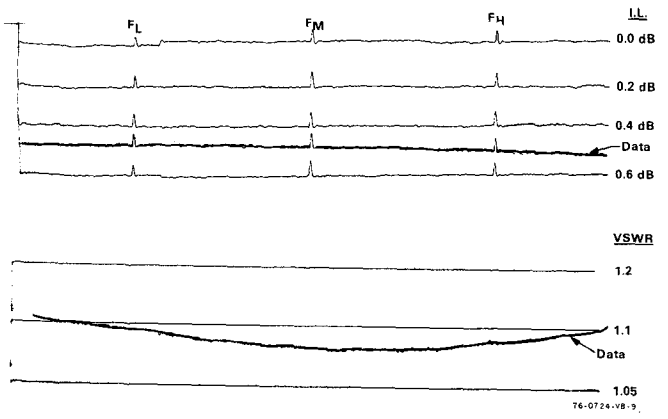

Figure 9. RP/STC SN 07 Insertion Loss and VSWR

Parameter	Value
Frequency	L-band (20% bandwidth)
RF Power Handling	200 watts Peak, 10% Duty
Operating Temperature	-55°C to +70°C
VSWR	1.2 *max*
Insertion Loss on Receive	0.5 dB max
Leakage Power (Passive)	<30 mW Peak Spike <20 mW Peak Flat
Leakage Power (with STC Gated)	<1 mW Peak
3-dB Recovery Time (Gated or Ungated)	<1 μs
STC Attenuation	0 to 20 dB
STC Turn-on and Turn-off Time	<0.2 μs
STC Driver Power Supply Voltages	+35 Vdc, -15 Vdc

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Figure 10. Receiver Protector Data

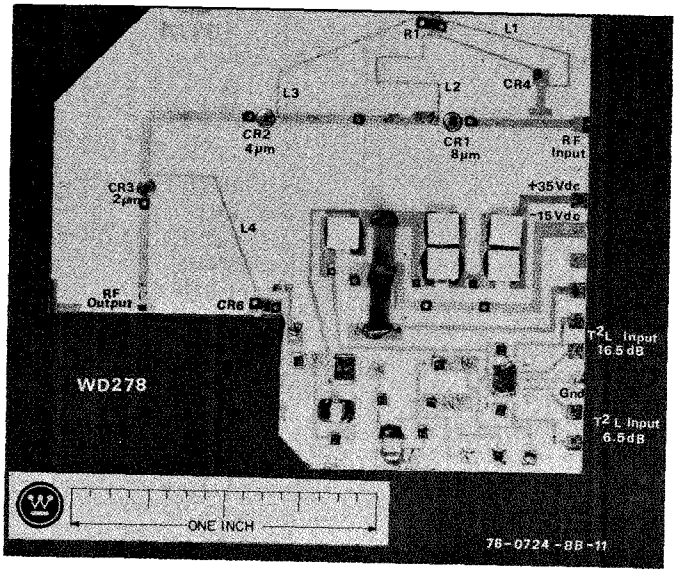

Figure 11. Receiver Protector/STC/Driver